### **Project: Two-Stage OTA (Operational Transconductance Amplifier)**

**Technology**: 180 nm (GPDK180)  
 **Design Platform**: Cadence Virtuoso  
 **Process**: CMOS Analog Design

### **Specifications**

* **Process Parameters**:  
  + Kn′=300 μA/V2K'\_n = 300\ \mu A/V^2Kn′​=300 μA/V2
  + Kp′=75 μA/V2K'\_p = 75\ \mu A/V^2Kp′​=75 μA/V2
  + VTN=−VTP=0.5 V V\_{TN} = -V\_{TP} = 0.5\ VVTN​=−VTP​=0.5 V or 0.35 V0.35\ V0.35 V
* **Design Requirements**:  
  + Load Capacitance, CL=2 pFC\_L = 2\ pFCL​=2 pF
  + DC Gain ≥ 60 dB
  + Gain Bandwidth Product (GBW): 30 MHz
  + Phase Margin ≥ 60°
  + Slew Rate: 20 V/μs
  + Power Dissipation ≤ 300 μW
  + ICMR (Input Common Mode Range):  
    - Max: 1.6 V
    - Min: 0.8 V
  + Power Supply: ±1.8 V

### **Transistor Dimensions**

| **Transistor** | **Width (W)** | **Length (L)** |
| --- | --- | --- |
| M1, M2 | 3 μm | 500 nm |
| M3, M4 | 7 μm | 500 nm |
| M5, M8 | 6 μm | 500 nm |
| M6 | 87 μm | 500 nm |
| M7 | 37.5 μm | 500 nm |

### **Other Parameters**

* Bias Current Is=20 μAI\_s = 20\ \mu AIs​=20 μA
* Compensation Capacitance Cc=800 fFC\_c = 800\ fFCc​=800 fF

### **Simulation Goals**

* Validate **gain**, **phase margin**, **GBW**, and **slew rate** using AC and transient simulations.
* Confirm **ICMR** via DC analysis.
* Verify **power dissipation** under nominal biasing.